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A novel method based solely on field programmable gate array (FPGA) units enabling measurement of time and charge of analog signals in positron emission tomography (PET)

Abstract: This article presents an application of a novel technique for precise measurements of time and charge based solely on a field programmable gate array (FPGA) device for positron emission tomography (PET). The described approach simplifies electronic circuits, reduces the power consumption, lowers costs, merges front-end electronics with digital electronics, and also makes more compact final design. Furthermore, it allows to measure time when analog signals cross a reference voltage at different threshold levels with a very high precision of ~15 ps (rms) and thus enables sampling of signals in a voltage domain.

Keywords: FPGA; TDC; TOF-PET.

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Introduction

The subject of this article is focused on the application of a novel measurement method of analog signals and its electrical parameters in time-of-flight positron emission tomography (TOF-PET) [1–3]. PET is used to determine the spatial and temporal density distribution of selected substances in the body. PET detectors register γ quanta originating from the annihilation of the positrons with electrons. Positrons are emitted by the radioisotopes included in the radiopharmaceuticals administered to the patient before the diagnosis.

The core of the PET scanner comprises scintillators converting the energy of annihilation quanta into light pulses that are subsequently converted to electrical signals by means of photomultipliers or photodiodes. These signals (in the case of TOF-PET [1–3]) have typically ~2 ns width and amplitude up to −6 V. To measure time and charge of such signals, one has to use a set of electronic circuits, which allow to discriminate (analog discriminators) and convert time to digital information [time to digital converter (TDC)]. Analog discriminators can be divided into constant-level or constant-fraction. In connection with TDC, they allow measurement of the time, at which the signal exceeds the preset voltage or a desired fraction of the amplitude, respectively. Discriminators and TDCs play a particularly important role in the latest generation of positron emission tomographs (so-called TOF-PET), which utilize information about a difference in TOF between the annihilation point and the detector for the two registered γ quanta.

Typical discriminators are built on the basis of standard electronic components and include, among other things, current source, preamplifier, comparator, shaper,

capacitors, resistors, diodes, transistors, and transmission lines. In the case of TDC, a dedicated application specific integrated circuit (ASIC) is used.

In this article, a novel solution is presented, which allows to incorporate discrimination and TDC into a field programmable gate array (FPGA) unit. For this purpose, low-voltage differential signal (LVDS) buffers of the FPGA device are used as a comparator [4] and internal carry-chain elements as delay elements.

FPGA-TDC

The time measurement technique in FPGAs is based on the possibility of using carry-chains usually used as part of adders [5, 6]. Carry-chain lines, because of its nature (adding long words), have minimized delay (in order to increase the possible maximum operating frequency of the FPGA).

As shown in Figure 1, time measurement is based on writing a bit vector, which represents STOP signal (measured signal), in the D-type flip-flops with the rising edge of the START signal (system clock). STOP signal is delayed by the elements of carry-chain, which normally is used by adders in an FPGA. The lower latency of a single element of the carry-chain translates to better precision of a time measurement.

To achieve the high precision of time measurement, one should take into account the influence of TDC integral nonlinearity, temperature, and supply voltage. Corresponding corrections can be calculated and added offline or in real-time to the measured values. Another difficulty is the so-called metastability resulting from different reaction time to the transition of the signal. When saving the current state of the STOP signal, it may be a case when there is no continuity of ones and zeros on the rising/falling edge of the measured signal (Figure 2).

Discontinuity of ones and zeros can also result from the different path lengths of carry-chain to the flip-flops. This, however, can be limited by writing appropriate constraints placing the individual elements (carry-chains and flip-flops) in the FPGA. As a result, in order to correctly decode binary sequence to time, the required amount of logic must be increased.

The first mentioned TDC technique was already implemented in a Trigger Readout Board version 3 [7]. As shown in Figure 3, it consists of five-lattice ECP3-150 FPGAs and there are no dedicated TDC components [such as HPTDC (http://tdc.web.cern.ch/tdc/hptdc/hptdc.htm)]. Therefore, four of them are foreseen to perform TDC on incoming signals. Board serves 256 TDC channels with ~10 ps time resolution. It is possible to synchronize TRB3 with other boards by means of reference signal measurement (each FPGA has one additional TDC channel). The fifth FPGA is responsible for the management of the data flow.

FPGA LVDS input buffer as a discriminator

FPGA LVDS buffer is typically used as buffer for digital signal transmission. When positive signal is higher than negative, it gives logical "1" and in opposite case "0". It should be noted that the input voltage range is limited to the acceptable voltage of FPGA LVDS buffer (usually from 0 to ~2 V). In our approach, an input signal will be split passively to four signals and its DC level will be moved to +2 V. Hit rate will be on the level of ~17,000/s for the whole detector (up to 240 scintillators). These working parameters allow to use it as a discriminator for TOF-PET signals.

In order to verify the applicability of FPGAs as discriminator, preliminary measurements were made. In Figure 4, a block diagram of the measurement setup is shown. A reference voltage signal (a 25 ns rising edge from
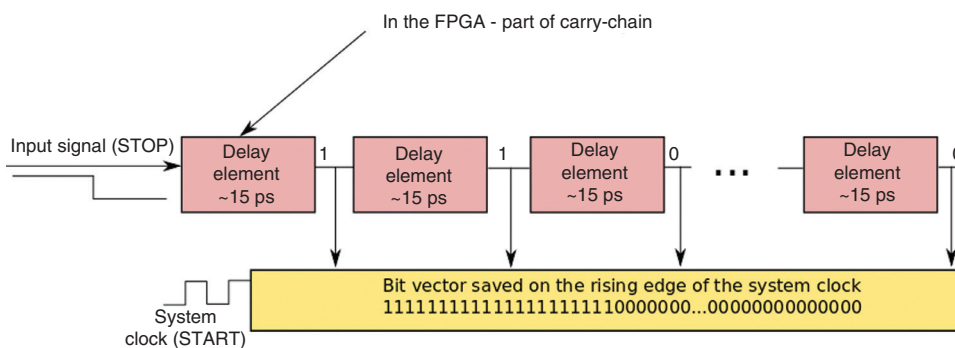

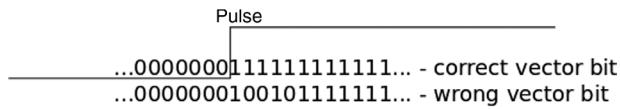**Figure 1**   Diagram of time measurement when using a carry-chain as a delay line.

Figure 2 Saved value in flip-flops may be not correct due to metastability.
Therefore, the amount of logic required to decode the time increases.

0 to 2 V) is supplied to one of the LVDS buffer differential inputs (+), while a constant level voltage is supplied to the other input. On the second LVDS buffer, a reference signal was connected. It indicated the beginning of the reference signal. In the FPGA, two TDC channels were implemented. With the increase of the voltage level, the time difference between the reference signal and the measured signal should also increase (Table 1 and Figure 5). Measured distribution of the time difference corresponds to the achievable discriminator resolution.

It should be emphasized that the results were achieved without any calibration. The time measurement precision achievable with FPGA-LVDS buffers together with FPGA-TDC is sufficient for the needs of the TOF-PET tomography (70 ps precision is acceptable). It can be noticed that, for lower signal amplitudes, one gets worse time resolution. It seems that this depends on the FPGA-LVDS buffer specific behavior and it should be investigated more thoroughly.

FPGA-ADC and FPGA-discriminator in TOF-PET application

When combining FPGA-TDC and FPGA-discrimination, one can sample incoming signal with very high precision (10 ps rms), which is particularly important in the case of TOF-PET based on the plastic scintillators [1–3], with the time of the rising edge of registered signals in the range of few nanoseconds. In order to perform sampling, the input signal is split into several ones, which are treated independently. The thresholds for the split signals can be adjusted depending on different conditions (baseline level and maximum signal amplitude; see Figure 6). Sampling may improve the time resolution significantly. This may be achieved, for example, by fitting a function describing the shape of the signals to sampled points (see Figure 6, red line), with the beginning of the measured signal as a free parameter of the fit. In addition, combination of rising and
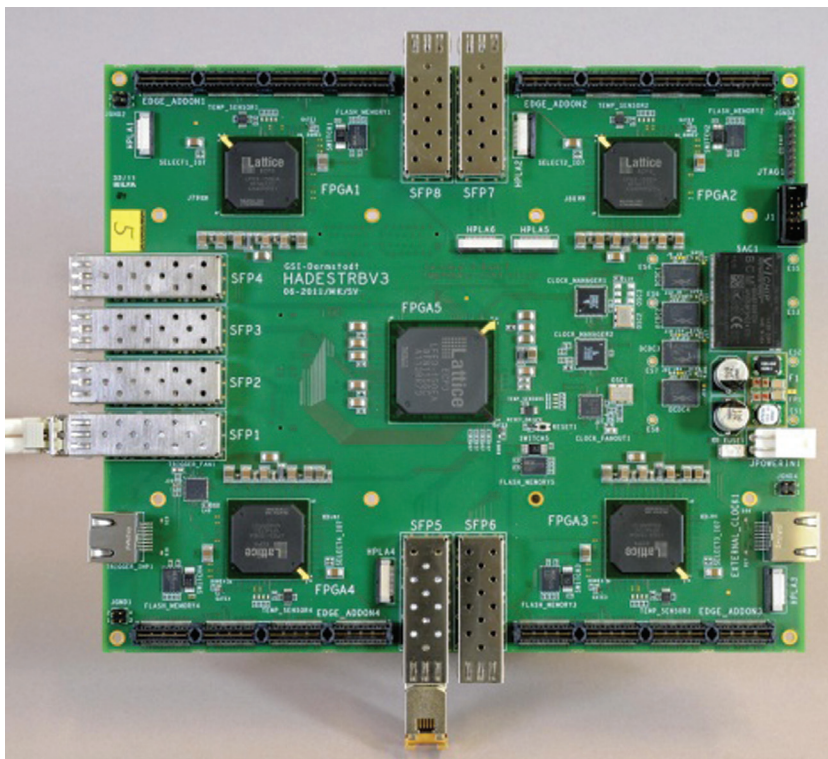

Figure 3 TRB3 for time measurements.
Four-lattice FPGAs placed in the corners of the board are used for time measurements. The central one is used for data flow management.
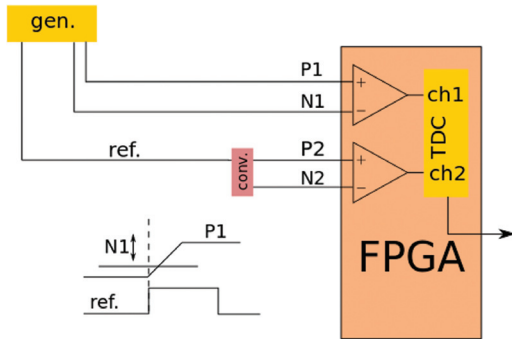
Figure 4 Test setup for measuring ADC-TDC performance.

Table 1 Results from ADC-TDC measurements.

N level, mV	Tome, ps	Jitter (RMS), ps
400	2551	50
800	3034	24.00
1200	3535	18.00
1600	4125	15.00

Figure 6 Scheme of a four-threshold device for the sampling in the voltage domain and the pictorial explanation of its functioning. ADC and TDC mixture increases resolution of time and amplitude measurement. The number of threshold can be increased according to the needs.

falling edges should allow for the measurement of charge with very good resolution (below 70 ps rms for TOF-PET). Charge measurement can be later on used for rejection of noise originating from registration of γ quanta scattered in the body of the patient.

Conclusions and discussion

Currently, TDC and charge-Q to digital converter (QDC) devices are widely used in the research as well as in the various types of diagnostic devices. Typically, time measurement is performed by dedicated ASICs (http://tdc.web.cern.ch/tdc/hptdc/hptdc.htm.) with the precision of up to about 20 ps (rms), and in the case of charge, an accuracy of <1% is achievable. However, in these cases, each time circuit (converter) has to be readout and their parameters have to be controlled by the peripheral devices. Most often, this is done by using microcontrollers or FPGAs.
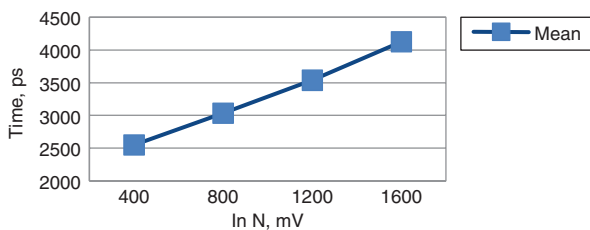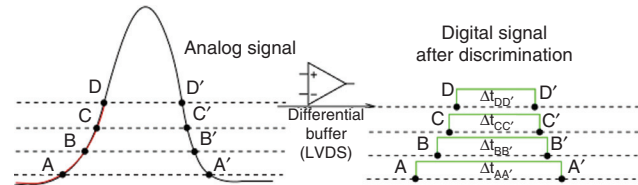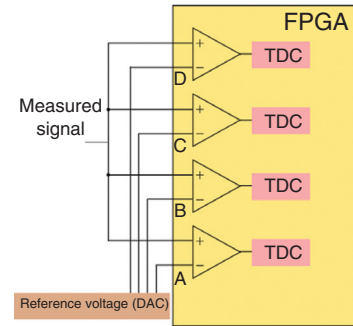

Figure 5 Measured time versus input voltage.

In this article, a novel method of the time measurement was presented, which allows for sampling of analog signals in the voltage domain with a precision of 10 ps (rms). The method is based on the usage of LVDS buffers of the FPGA device as a comparator and internal carry-chain elements as delay units. It is developed for the purpose of sampling of fast signals in the newly developed TOF-PET detector system based on the plastic scintillators.

The benefits from presented measurement techniques integrated within FPGA are as follows:

– Reduction of cost of measurement systems – no need to purchase a dedicated ASIC (cost is reduced by ~$10 per channel),
– Low power consumption (only FPGA and discrete components; ~100 mW smaller power consumption per channel),
– Much higher concentration of measurement channels compared to the traditional approach (up to 256 channels per TRB3 board),
– Much more flexibility and possibility of miniaturization of the measurement systems, and
– Possible use in other readout systems where sampling of fast signals is required.

Conflict of interest statement

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