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GASTONE64: A new front-end ASIC for the cylindrical GEM Inner Tracker of KLOE-2 experiment at DAΦNE

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ABSTRACT

GASTONE64 (Gem Amplifier Shaper Tracking ON Events) is a novel 64-channel mixed analog-digital ASIC developed to readout the cylindrical GEM inner tracking detector of the KLOE-2 apparatus at the e^+e^- DAΦNE collider. It has been designed in the CMOS 0.35 μm technology and each analog channel is made of preamplifier, shaper and discriminator. The expected input charge ranges between few fC up to 40 fC, the charge sensitivity is 16 mV/fC while the equivalent input noise charge (ENC) is 800 e^-+40 e^-/pF. The discriminated signals are read-out using a 100 MBit/s LVDS serial data link. The power consumption is about 6 mW/channel.

1. Introduction

An Inner Tracker based on a fully cylindrical triple GEM detector (CGEM) is under construction for the upgrade of the KLOE apparatus at the DAΦNE Φ factory, in order to improve the vertex resolution and vertex reconstruction capability [1]. It consists of four concentric cylinder detectors with a total material budget of ~2% X_0 and a diameter ranging between 260 mm and 460 mm (Fig. 1).

The anodic readout plane of each CGEM is segmented with *X*–*V* patterned copper strips with a stereo angle of 40°, for a total of about 30,000 readout channels. The *X* strips, providing the r–ϕ coordinate, have a pitch of 650 μm, a fixed length of 694 mm and 250 μm width with total capacitance *C*~100 pF. The *V* strips, made of *V*-pads connected through vias, provide the *z* coordinate and their length ranges between 1 mm and 773 mm with a capacitance ranging between 1 and 200 pF. Such large variations in parasitic capacitance prevented the *S*/*N* optimization based on shaping filter fine tuning. The overall spatial resolution is $\sigma_{r\phi} = 200$ μm and $\sigma_z = 500$ μm. The strip signals are read-out through 120-pin connectors, each one collecting groups of 40 *X* strips and 80 *V* strips. In Fig. 2 the *X*–*V* plane implementation of the readout plane is shown. The quality control of the anodic signal plates has been performed using a method based on reflected signal analysis procedure, implemented on a cost effective FPGA [2]. This test system is capable to find out defects of the readout plane, either short circuits or interruptions, through the search of discontinuities in the impedance profile of the transmission line. The device can measure the time difference between injected and reflected signal with a precision of 100 ps, allowing to localize a defect within about 1 cm.

2. GASTONE64

A novel mixed analog-digital front-end chip has been developed to fulfil the constraints imposed by the KLOE-2 Inner Tracker detector. In particular, due to the limited gas amplification featured by the GEM, the expected input charge ranges from a few fC to some tens of fC. The second constraint comes from the high

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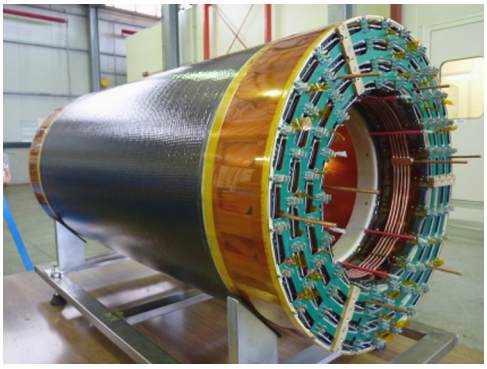

Fig. 1. KLOE2 Inner Tracker.

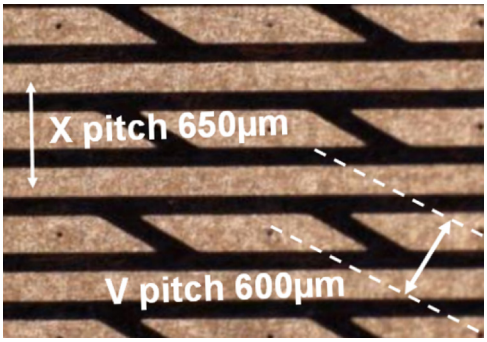

Fig. 2. XV readout implementation.

density of readout strips, leading to design a circuit with 64 channels, serial readout (to minimize the number of input/output connections) and low power consumption. The expected event rate on the innermost layer will not exceed 30 kHz/strip, thus a DC baseline restoration circuit to limit baseline fluctuation is not strictly required. Considering that the expected background is negligible, a deep sub-micron technology was not mandatory and the relatively cheap 0.35 μm CMOS technology was considered fully adequate. After a 16-channel prototype [3], the 64-channel version has been designed and produced. Its layout is shown in Fig. 3 while its block diagram is shown in Fig. 4.

2.1. The analog section

The analog channel architecture is made of four blocks: a charge sensitive preamplifier, a shaping stage, a leading-edge discriminator and a monostable circuit. The charge sensitive preamplifier integrates the input current signal from the readout electrodes into a voltage. Its main characteristics are charge sensitivity of 3 mV/fC @C_{IN}=100 pF, a non-uniformity less than 1% (0–50 fC input range) and a supply current of about 280 μA. The amplifier-shaper provides noise filtering and semi-gaussian shaping. Its supply current is about 150 μA, the overall peaking time is 90 ns @C_{IN}=100 pF, while the charge sensitivity is 16 mV/fC @C_{IN}=100 pF. The shaper is followed by a leading-edge discriminator that generates the digital tracking information. Finally, the monostable stretches the digital signal to store the information awaiting for the experiment trigger signal, with a programmable pulse width ranging between 200 ns and 1 μs. Fig. 5 shows the output of the shaper on a test pin for a 20 fC input test pulse.

2.2. The digital section

The digital section contains both a slow-control and a readout logic. The slow-control section consists of a SPI interface port

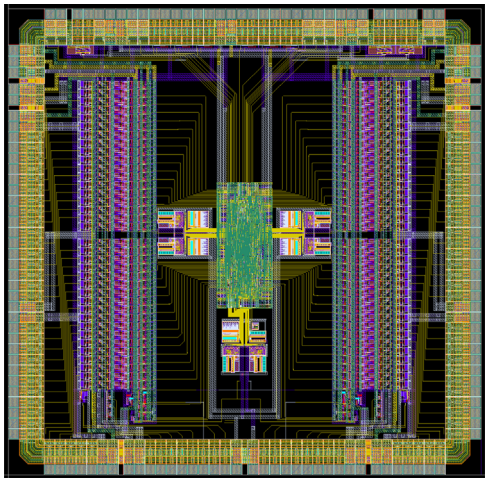

Fig. 3. GASTONE64 layout.

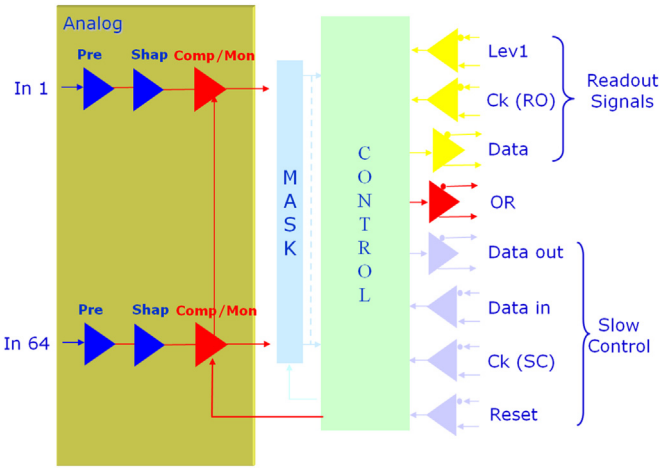

Fig. 4. GASTONE64 block diagram.

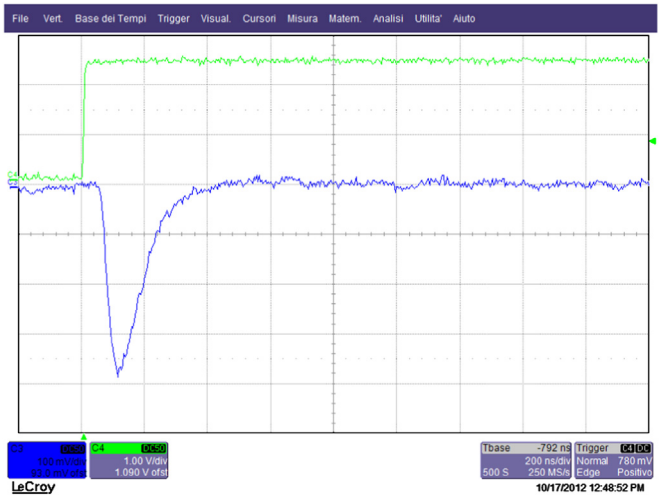

Fig. 5. Shaper response for 20 fC input pulse.

running at 1 MHz, controlling the read–write operations on the internal DACs used for threshold, pulse width and test input settings, together with the mask registers and some other configuration registers (there are 28 8-bit registers in total). The readout section controls the serialization of the 64 digital output signals

Table 1
Main chip characteristics.

N channels	64
Chip dimensions	4.5×4.5 mm^2
Input impedance	120 Ω
Charge sensitivity	16 mV/fC (C_{det} = 100 pF)
Peaking time	90 ns (C_{det} = 100 pF)
Crosstalk	< 3%
ENC	800 e$^-$+40 e$^-$/pF
Power consumption	~6 mW/ch
Readout	Serial LVDS (100 Mbps)

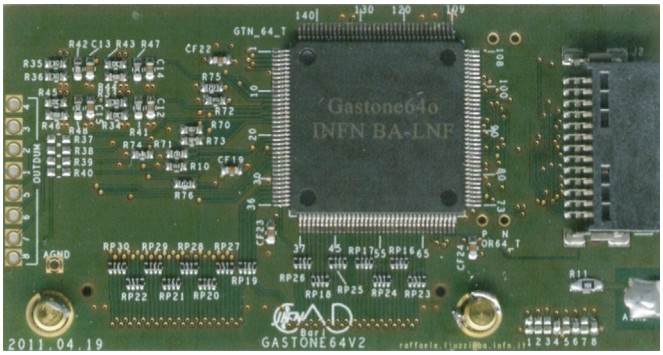

Fig. 6. Front-end board picture.

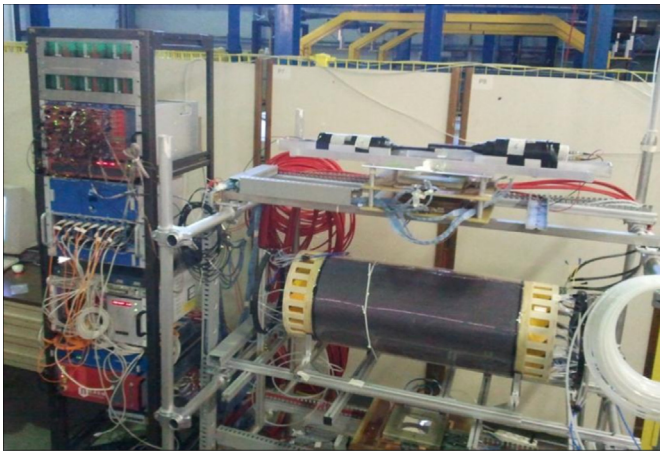

Fig. 7. Layer2 CGEM at cosmic-ray test stand.

and the readout protocol. Upon the arrival of the trigger, the signals coming from the analog section are stored into the transmission shift register and the Readout electronics sends exactly the number of clock cycles needed to read it. Each 96-bit event word contains a 10 bits header, 5 bits identifying the trigger number, 9 bits for chip ID, 64 bits for data and 8 bits at 0 ending the data-frame. The readout is performed using both edges of a 50 MHz clock, thus at 100 MBit/s, through a single LVDS output line. The clock will be running only during the readout phase to minimize interferences with the analog section. The chip also produces a global OR signal for self-triggering application purpose. Its main characteristics are summarized in Table 1.

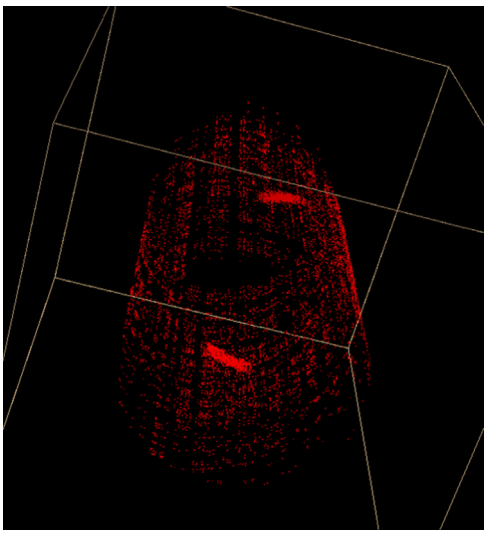

Fig. 8. Event display of Layer2 CGEM.

3. Validation tests

A very compact Front-End Board (75×40 mm^2) housing two GASTONE64 chips has been developed, produced and tested (Fig. 6) using an automatic test bench.

GASTONE64 has been mounted on the cylindrical GEM for the final validation before the installation in the KLOE apparatus. The tests have been carried out by using an acquisition system based on a customized version of the General Interface Board (GIB) developed for the KLOE DAQ upgrade [4]. The GIB board has been customized to set-up the frontend chip parameters, deliver the power supply and download data from eight GASTONE front-end cards through a serial interface for a total of 960 channels. The acquired data are then sent through a 2 Gb/s Optical port to the Read Out Driver card (ROD), which performs the first level event-building. A VME CPU board collects data from the ROD and sends them to the farm on-line system. Fig. 7 shows the Layer2 equipped with GASTONE64 at the cosmic-ray test stand, where the trigger is built with 4 scintillators and an external tracking system made of 3 planar GEMs to improve the selection of cosmic-ray muon tracks. An event display is shown in Fig. 8.

4. Conclusions

A novel 64 channels ASIC, named GASTONE64, has been developed to read out the KLOE Inner Tracker detector based on cylindrical GEM at DAΦNE. The new chips fulfill all the required specifications. Its production has already been carried out and the installation on the KLOE Inner Tracker is going on.

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